

Parametric Measurement Unit (PMU) Layout Guidelines

This application note discusses ways to help system designers apply proper layout techniques and signal routing. The layout and component descriptions will minimize noise pick-up and manage the thermal dissipation in applications using PMUs.

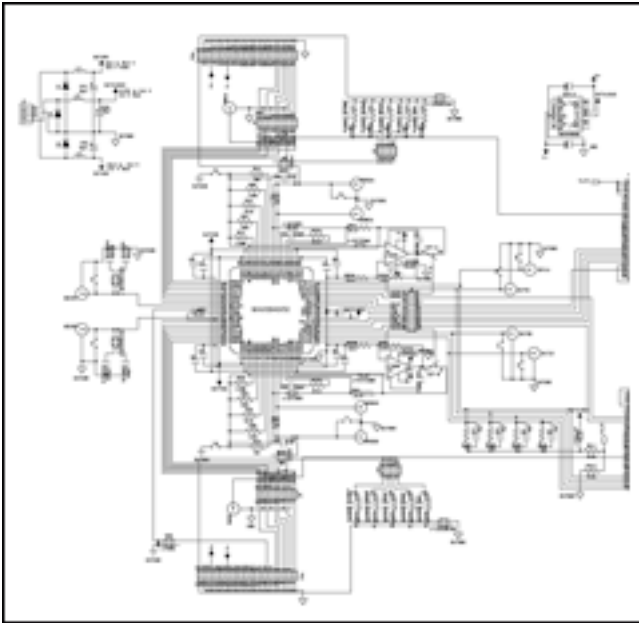
Introduction

As with all precision electronic circuits, the proper choice of supporting components and layout will ensure the best performance possible. This application note will describe the circuit, compensation, layout, and thermal management requirements of the MAX9949/MAX9950 PMU.

Device Description

The MAX9949/MAX9950 are dual PMUs intended for ATE and other instrumentation. Their small size, wide force and measure range, and high accuracy make the MAX9949/MAX9950 ideal for testers that require a PMU per pin or per site. The MAX9949/MAX9950 have a built-in external buffer-drive feature that can be used to expand the voltage and current range of the PMU, depending on the user's application.

Typical Circuit



[For Larger Image](#)

Suggested Circuit Layout

Use a multilayer PCB with separate power and ground planes. Use 1oz copper for the power and ground. The power plane may be shared for the VCC, VEE and VL levels, if board layers are at a premium. Note: AGND should be kept quiet as it is the ground for the internal references. Digital currents should not flow through the AGND power plane near the analog inputs. The best solution is to have a split ground plane for AGND and DGND. With careful board layout, however, the grounds may be shared.

Place the main amplifier-compensation capacitor, C_{CM} , close to the PMU to minimize parasitics. (Refer to block diagram in the MAX9949/50 data sheet.)

Power Supplies

Power-supply connections should be bypassed with good high-frequency capacitors positioned close to the PMU pins. In most cases 0.1 μ F ceramic capacitors should be used. The MAX9949/MAX9950 can supply currents as high as 25mA into a load. Applications with low impedance loads or capacitive loads demand large currents from the power supplies. Shared 1 μ F bypass capacitors per every four to six PMUs will improve the dynamic performance in these applications.

Main Amplifier

The main amplifier in the PMU is designed to be stable with loads up to 2500pF when compensated with a 120pF capacitor. Faster rise times are possible with smaller main-amplifier compensation at the cost of longer settling times.

Thermal Management

The MAX9949/MAX9950 are housed in a 64-TQFP thermally enhanced package. The user can choose between two package options, exposed pad on top -EPR or bottom -EP.

In applications where the heat is conducted to the bottom of the package, the thermal attach pad on the board should be made on the top trace layer. Note: the exposed pad is electrically connected to the most negative supply of the chip (VEE). This pad must either be connected to VEE or floated—**DO NOT TIE THE EXPOSED PAD TO ANY OTHER ELECTRICAL POINT**. The attach-pad width and length dimensions are to be no more than 1mm greater than the corresponding width and length dimensions of the thermal attachment structure. (Consult EIA/JEDEC standard JESD51-5 & JESD51-7 for further details.)

In applications where the heat is conducted to the top of the package, active cooling is recommended. Contact the top of the package with either a forced liquid-cooled silicone bladder or a water-/liquid-cooled cold plate. Again, the exposed pad is electrically connected to VEE.

Conclusions

Proper choice of support components and layout will allow the user to deliver the most accurate and efficient performance from the PMU for their end application.

More Information

MAX9949: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)

MAX9950: [QuickView](#) -- [Full \(PDF\) Data Sheet](#)